



Patent Application
Attorney Docket No.: 57941.000063
Client Reference No.: RA001.2003.2.C.US

JRW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: :
: Michael FARMWALD et al. :
: Group Art Unit: 2818
Appln. No.: 10/716,596 :
: Examiner: Unassigned
Filed: November 20, 2003 :
: For: INTEGRATED CIRCUIT I/O USING :
: A HIGH PERFORMANCE BUS :
: INTERFACE :

MAIL STOP AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with the duty under 37 C.F.R. § 1.56 of each individual associated with the filing and prosecution of the above-identified patent application (hereinafter, "associated individuals") to disclose all information known to that individual to be material to patentability, Applicant(s) hereby submits attached Form PTO-1449 (modified) listing cited references. This submission is made in accordance with 37 C.F.R. §§ 1.97 and 1.98 and § 609 of the Manual of Patent Examining Procedure.

The cited references, while believed to be of some relevance, are not necessarily considered to teach or suggest any aspect of the invention described and claimed in the above-

identified patent application. Applicant(s) hereby expressly reserves the right to swear behind the effective dates of any of the cited references. Applicant(s) further reserves the right to question the relevance, materiality, and/or prior art status of any of the cited references in whole, in part, or in combination, subsequent to the filing of this information disclosure statement. This information disclosure statement is also not to be construed as a representation that a search has, or has not, been conducted or that no better art exists. Rather, this information disclosure statement discloses only the best references of which the associated individuals are aware.

The Examiner is respectfully requested to consider each of the cited references, to indicate such consideration by initialing in the space provided next to each cited reference on the enclosed Form PTO-1449 (modified), to sign the initialed Form PTO-1449 (modified), and to return a copy of the same with the next communication to the Applicant(s).

For the convenience of the Examiner in considering the cited references, a copy of each of the cited references is enclosed with this communication. In considering the cited references, it may be noted by the Examiner that certain of the references may contain markings, underlinings, and/or other notations. These markings, underlinings, and/or other notations

are not to be construed as drawing the Examiner's attention either to selected parts or away from other parts of the cited references. Any such markings were either present on the copies of the cited references obtained by the associated individuals, or were made thereon during the study of the references by the associated individuals.

In accordance with 37 CFR § 1.97(b), this information disclosure statement is being filed (i) within three months of the filing date of the above-identified patent application; (ii) within three months of the date upon which the above-identified patent application entered the national stage as set forth in 37 CFR § 1.491; or (iii) before the mailing date of a first Office Action on the merit for the above-identified patent application. Accordingly, no statement or fee is required.

Please charge any shortage in fees due in connection with the filing of this communication to Deposit Account No. 50-0206, and please credit any excess fees to such deposit account.

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Respectfully submitted,

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FORM PTO-1449 (REV. 7-80)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO.: 57941.000063		SERIAL NUMBER: 10716,596	
<div style="text-align: center;"> LIST OF MATERIALS CITED BY APPLICANT (Use several sheets if necessary) Page 1 of 1 </div>				APPLICANT(S): MICHAEL FARMWALD et al.		GROUP ART UNIT: 2818	
				FILING DATE: November 20, 2003			

OIP
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 PATENT & TRADEMARK OFFICE

U.S. PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	1.	5742798	04-21-1998	Goldrian			
	2.	4480307	10-30-1984	Budde et al.			

FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS AND SUBCLASS	TRANSLATION PROVIDED	
						Yes	No
	3.	2000035831 A	02-02-2000	JP		X (Abstract)	
	4.	0 348 113 A2	12-27-1989	EP			X

OTHER MATERIALS (Including Author, Title, Date, Pertinent Pages, Etc.)	
5.	Opposition against European patent 0 525 068, (Application No. 91 908 374.1-2201) (German & English Translation), 04-15-2004
6.	Communication of the Technical Board of Appeal 3.5.1 pursuant to Article 11 (1) of the rules of procedure of the Boards of Appeals in the Opposition against European patent 0 525 068 (Application No. 91908374.1-2201), 11-20-03
7.	Brief Communication in the Opposition against European patent 1 022 642 (Application No. 00108822.8), 04-16-2004
8.	Minutes of the oral proceedings of February 10, 2004 in the Opposition against European patent 0 525 068, 02-18-2004
9.	LU et al., The Future of DRAMs, ISSCC 88, 02-18-2004, pp. 1-2
10.	Opposition against European patent 1022642, (Application No. 0010822.8) (German & English Translation), 03-02-2004
11.	Opposition against European patent 1004956, (Application No. 00010832.4) (German & English Translation), 03-03-2004
12.	Opposition against European patent 1022642, (Application No. 0010822.8) (German & English Translation), 07-15-2004
13.	Opposition against European patent 1004956, (Application No. 00010832.4) (German & English Translation), 07-15-2004
14.	Intel, iAPX 43204, iAPX 43205, Fault Tolerant Bus Interface and Memory Control Units, pp. 1-32, March 1983
15.	Intel, Electrical Specifications for iAPX 43204 Bus-Interface Unit (BIU) and iAPX 43205 Memory Control Unit (MCU), March 1983
16.	Intel, Memory Components Handbook, 1985
17.	Summons To Attend Oral Proceedings Pursuant to Rule 71(1) EPC in the Opposition against European patent 1 004 956, 07-20-04
18.	HUBER, Expert Report Regarding the Invention Claimed in Rambus' EP 0 525 068 Patent vs. The CVAX CMCTL—A CMOS Memory Controller Chip and Designing Memory Systems with the 8K x 8 iRAM, July 13, 2004
19.	Decision of February 12, 2004 by the Board of Appeals of the EPO in the Opposition against European patent 0 525 068 (Application No. 91908374.1)
20.	MORGAN, The CVAX CMCTL — A CMOS Memory Controller Chip, Digital Technical Journal, No. 7, August 1988, pp. 139-143
21.	FELLIN et al., Intel, Application Note, AP-132, Designing Memory Systems with the 8K x 8 iRAM, June 1982
22.	PRINCE et al., Semiconductor Memories, A Wiley-Interscience Publication, 1983
23.	Decision of the Technical Board of Appeal 3.5.1 of February 12, 2004 in the Opposition against European patent 0 525 068 (Application No. 91908374.1-2201/0525068)

EXAMINER	DATE CONSIDERED
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.